REMARKS

Claims 1-20 are pending in the present application. Claims 1-20 are rejected in the present Office Action. By this response, claims 1, 7, and 14-18 are amended. In view of the above amendments and the following discussion, Applicants submit that none of the claims now pending in the application are unpatentable under 35 U.S.C. §§101, 112, or 103. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. REJECTION OF CLAIMS FOR NON-STATUTORY DOUBLE PATENTING

Claims 14-17 are rejected on the grounds of non-statutory double patenting over claims 1-2 of U.S. Patent 7,185,309 and claims 1-6, 10-16, and 24 of U.S. Patent 7,228,520. (Office Action, p. 3). Applicants file herewith a terminal disclaimer over U.S. Patents 7,185 ,309 and 7,228,520. Accordingly, Applicants respectfully request that the present rejection be withdrawn.

II. REJECTION OF CLAIMS UNDER 35 U.S.C. §112

Claims 8-9 and 15-17 are rejected under 35 U.S.C. §112 as being indefinite. In particular, the Examiner stated that the phrases "said multithreading system" in claim 8, and "the system" in claims 15-17, lack antecedent basis. (Office Action, p. 4). With respect to claim 8, Applicants note that claim 7, from which claim 8 depends, includes the phrase "a multithreading system". That is, claim 7 recites "generating a physical description of a multithreading system...." Therefore, the phrase "said multithreading system" in claim 8 has antecedent basis in claim 7. Applicants assume claim 9 was rejected for its dependence from claim 8, since no specific rejection of claim 9 is given in the Office Action. With respect to claims 15-17, Applicants have amended the preambles thereof to recite "The design tool of...," which finds antecedent basis in independent claim 14.

Accordingly, Applicants contend that claims 8-9 and 15-17 are definite and, as such, fully satisfy the requirements of 35 U.S.C. §112. Applicants respectfully request that the present rejection be withdrawn.

III. REJECTION OF CLAIMS UNDER 35 U.S.C. §101

Claims 14-17 and 18-20 are rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. In particular, it was stated that claims 14-17 are directed to a "design tool" which would be reasonably interpreted by one skilled in the art as "software per se." (Office Action, p. 5). The Examiner further states that claims 18-20 would also be considered "software per se." (Office Action, p. 5). The rejection is respectfully traversed.

With respect to claims 14-17, Applicants have amended claim 14 to recite some features in means-plus-function language as permitted by 35 U.S.C. §112, sixth paragraph. In particular, Applicants' claim 14 recites a means for specifying attributes of said multithread message process system, a means for generating a plurality of instances of said thread model and an instance of said interconnection model in response to said specified attributes, and a means for implementing said plurality of thread model instances and said interconnection model instance in terms of said integrated circuit architecture. The sixth paragraph of §112 states that means-plus-function language "shall be construed to cover the corresponding structure...described in the specification and equivalents thereof." Applicants disclose a computer that includes a CPU, support circuits, and a memory. The memory stores software, which is capable of executing circuit design process. (Applicant's specification, ¶¶0044-0047; Fig. 17). The Federal Circuit has held that a stored program in a digital computer is within the Section 112 paragraph 6 range of equivalents of a computer structure disclosed in the specification. In re Alappat, 35 USPQ2d 1545, 1558 (Fed. Cir. 1994) (en banc). Thus, claims 14-17 are not directed to "software per se" and are statutory within the meaning of 35 U.S.C. §101.

With respect to claims 18-20, Applicants claim 18 recites first and second configured portions of an integrated circuit. Since an integrated circuit is clearly a machine or apparatus within the meaning of 35 U.S.C. §101, a configured portion of such an integrated circuit is also a machine or apparatus. The Examiner has not provided any evidence that configuration portions of an integrated circuit are "software per se." As such, claims 18-20 are statutory.

Accordingly, Applicants contend that claims 14-17 and 18-20 fully satisfy the requirements of 35 U.S.C §101. Applicants respectfully request that the present rejection be withdrawn.

IV. REJECTION OF CLAIMS UNDER 35 U.S.C. §103

A. Claims 1-2, 5-8, 11-16, and 18

Claims 1-2, 5-8, 11-16, and 18 are rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent Application Publication 2005/0038806 by Ma in view of U.S. Patent 6,704,914 issued to Nishida et al. ("Nishida"). The rejection is respectfully traversed.

With respect to Applicants' claim 18, the Examiner stated that Ma teaches Applicants' first and second configuration portions of an integrated circuit as recited therein, with the exception of the use of thread circuits. (Office Action, p. 6). The Examiner stated that Nishida teaches generating thread circuits coupled to control logic. (Office Action, p. 7). The Examiner concluded that it would be obvious to combine the thread circuits of Nishida with the system of Ma to render obvious Applicants' claim 18.

Applicants have amended claim 18 to more particularly point out and distinctly claim the invention. In particular, the second configured portion within the integrated circuit provides a connection between threads, and the connection includes at least one control signal provided by the control logic of one of the threads. (See Applicants' specification, para. [0109]). The combination of Ma and Nishida does not teach or suggest such a connection between thread circuits in a second configuration portion of an integrated circuit.

Notably, Ma generally teaches the concept of multi-threaded programs and multi-threading. (Ma, Abstract). In FIG. 2, Ma shows multiple processors coupled to an interconnect, which is in turn coupled to a memory controller and a memory. However, Ma is silent with respect to how multiple threads are used in the system of FIG. 2. In particular, FIG. 2 of Ma does not show thread circuits with a connection that provides a control signal from control logic of one thread to another. In FIG. 3, Ma shows a logical conception of a multithreaded system, but does not show a specific

configuration of multiple thread circuits with a connection that provides a control signal from one thread to another.

Nishida generally teaches a synthesis technique for generating multi-threaded logic. (Nishida, Abstract). Nishida describes several example circuits where multiple threads access a common shared memory. (See Nishida, col. 5, lines 15-28; col. 9, lines 50-65; col. 11, lines 25-38; col. 15, lines 38-50). Nishida describes a "thread" as a circuit having an independent finite state transfer machine. (Nishida, col. 5, lines 20-23). Nishida, however, does not describe any connection mechanism between threads, other than the shared memory. In particular, Nishida does not teach or suggest thread circuits with a connection that provides a control signal from control logic of one thread to another.

As such, neither Ma nor Nishida teach or suggest thread circuits with a connection that provides a control signal from control logic of one thread to another. Thus, no permissible combination of Ma and Nishida renders obvious Applicants' invention recited in claim 18.

Applicants have amended claims 1 and 7 to include features similar to those emphasized above in claim 18. In particular, Applicants' claim 1 recites that each of the thread circuits provides a control signal to each other thread circuit through the interconnection topology. Applicants' claim 7 recites a connection between threads that includes at least one control signal provided by control logic of one of the threads. For the same reasons discussed above, the combination of Ma and Nishida fails to render obvious Applicants' invention of claims 1 and 7.

With respect to Applicants' claim 14, the Examiner asserted the same rationale to reject Applicants' claim 14 as Applicants' claim 7. Applicants' claim 14, however, includes different features than Applicants' claim 7. Notably, Applicants' claim 14 recites a first database for storing a multithread model having a thread model and an interconnection model, and a second database for storing an architecture of the integrated circuit. The Examiner did not cite any portion of either Ma or Nishida that teaches or suggests such databases. As such, there is no prima facie case of obviousness for Applicants' claim 14.

Claims 2, 5-6, 8, 11-13, and 15-16 depend, either directly or indirectly, from claims 1, 7, and 14. Since the combination of Ma and Nishida does not render obvious Applicants' claims 1, 7, and 14, the cited combination also fails to render obvious Applicants' claims 2, 5-6, 8, 11-13, and 15-16.

Accordingly, Applicants contend that claims 1-2, 5-8, 11-16, and 18 are patentable over the cited combination and fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the present rejection be withdrawn.

B. Claims 3-4, 9-10, 17, and 19-20

Claims 3-4, 9-10, 17, and 19-20 were rejected as being unpatentable over Ma and Nishida, in further view of U.S. Published Patent Application 2003/0126186 by Rodgers et al. ("Rodgers"). The rejection is respectfully traversed.

Claims 3-4, 9-10, 17, and 19-20 depend from claims 1, 7, 14, and 18 and recite additional features thereof. The cited combination does not teach, suggestion, or otherwise render obvious Applicants' claims 1, 7, 14, and 18. The deficiencies of Ma and Nishida with respect to claims 1, 7, 14, and 18 are described above. Rodgers generally teaches a technique for suspending execution of a thread until a specified memory access occurs. (Rodgers, Abstract). Rodgers does not teach or suggest thread circuits with a connection that provides a control signal from control logic of one thread to another. Since none of the cited references teaches or suggests such feature, no permissible combination thereof renders obvious Applicants' invention recited in claims 1, 7, 14, and 18.

Accordingly, Applicants contend that claims 3-4, 9-10, 17, and 19-20, which depend from claims 1, 7, 14, and 18, are patentable over the cited combination and fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the present rejection be withdrawn.

CONCLUSION

Claims 1, 7 and 14-18 have been amended. No new matter is introduced by entry of these amendments. Applicants submit that all of the claims presently in the application are allowable over the provisions of 35 U.S.C. §§101, 112, or 103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any action in any of the claims now pending in the application, it is requested that the Examiner telephone the undersigned at (408) 879-6149 (Pacific Time Zone) so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent & Trademark Office on April 2, 2009.

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